UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,173	12/31/2003	Tal Gat	P-6382-US	5558

49444 7590 09/05/2007

PEARL COHEN ZEDEK LATZER, LLP
1500 BROADWAY, 12TH FLOOR
NEW YORK, NY 10036

EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	**PAPER NUMBER**
2183	

MAIL DATE	DELIVERY MODE
09/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/748,173	GAT ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,6-8,11,12,14-16,20 and 22-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6-8,11,12,14-16,20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 4, 6-8, 11-12, 14-16, 20 and 22-25 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 8/3/2007.

Withdrawn Objections and Rejections

3. The 35 U.S.C. 112 second paragraph rejections are withdrawn due to amendment.

New Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-2, 4, 6-8, 11-12, 14-16, 20 and 22-25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1, 12, and 20 recite the limitation "delivering said branch predictions to an instruction fetch unit during the same two clock cycle period as it is stored in said queue." There is no support within the specification that the storing of the branch predictions generated takes two clock cycles. In the specification on page 7 lines 14-

20, it states "BPU 10 may start generating predictions for 100 and 101 in clock cycle T0, and by the end of T1 may complete the prediction, store the generated predictions ..." This shows that the storing of branch predictions takes a single cycle, T1 in this case. Also, for claims 12 and 20, there is no support for delivering both branch predictions to the instruction fetch unit in the same two clock cycle period. Figure 4 instead shows a single prediction being capable of being bypassed to the instruction fetch unit the same cycle that it's to be stored in the branch queue. Thus, the limitations "delivering said branch predictions" and "during the same two clock cycle period as it is stored in said queue" have no support in the specification at the time the application was filed. For examination purposes, the newly added limitation will not be examined.

6. Claims 2, 4, 6-8, 11, 14-16, and 22-25 are rejected due to their dependency.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-2, 4, 6-8, 11-12, 14-16, 20 and 22-25 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "delivering said branch prediction to an instruction fetch unit during the same two clock cycle period as it is stored in said queue." There is no support within the specification that the storing of the branch predictions generated takes two clock cycles. In the specification on page 7 lines 14-20, it states "BPU 10 may start generating predictions for 100 and 101 in clock cycle T0, and by the end of T1 may complete the prediction, store the generated predictions ..." This shows that the

storing of branch predictions takes a single cycle, T1 in this case. In addition, there's no antecedent basis for the limitation "said branch prediction," which will instead be interpreted as "a branch prediction." Thus, for examination purposes, the limitation will be interpreted as "delivering [[said]] a branch prediction to an instruction fetch unit during the same [[two]] single clock cycle period as [[it]] a branch prediction is stored in said queue"

Claims 12 and 20 recite the limitation "delivering said branch predictions to an instruction fetch unit during the same two clock cycle period as it is stored in said queue." There is no support within the specification that the storing of the branch predictions generated takes two clock cycles. In the specification on page 7 lines 14-20, it states "BPU 10 may start generating predictions for 100 and 101 in clock cycle T0, and by the end of T1 may complete the prediction, store the generated predictions ..." This shows that the storing of branch predictions takes a single cycle, T1 in this case. Additionally, there is no support for delivering both branch predictions to the instruction fetch unit in the same two clock cycle period. Figure 4 instead shows a single prediction being capable of being bypassed to the instruction fetch unit the same cycle that it's to be stored in the branch queue. Finally, there's no antecedent basis for the limitation "said branch predictions," which will instead be interpreted as "a branch prediction." Thus, for examination purposes, the limitation will be interpreted as "delivering [[said]] a branch prediction[[s]] to an instruction fetch unit during the same [[two]] single clock cycle period as [[it]] a branch prediction is stored in said queue"

9. Claim 1 recites the limitation "delivering said branch prediction" in line 10 of the claim. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 1, 12, and 20 recites the limitation "the same two clock cycle period" in line 11, lines 6-7, and lines 8-9 of the claims respectively. There is insufficient antecedent basis for this limitation in the claim.

11. Claims 2, 4, 6-8, 11, 14-16, and 22-25 are rejected due to their dependency.

Maintained Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 1-2, 4, 6-8, 11-12, 14-16, 20 and 22-25 are rejected under 35 U.S.C. §103(a) as being unpatentable over Reinman et al. ("Optimizations Enabled by a Decoupled Front-End Architecture"), in view of Giacalone et al. (U.S. 6,272,624), in view of Tran (U.S. 6,101,577).

14. As per claim 1:

Reinman disclosed a method comprising:

Storing said branch predictions in a queue (Reinman: Figure 5, sections 3 and 4.1 and 5.2)(Predictions are stored in the fetch target queue); and

Delivering a stored branch prediction from said queue to an instruction fetch unit (Reinman: Figure 5, sections 3 and 4.1);

Delivering a branch prediction to an instruction fetch unit during the same single clock cycle period as a branch prediction is stored in said queue (Reinman: Figure 5, sections 3 and 4.1)(It's obvious to one of ordinary skill in the art that a branch prediction stored in the queue could be delivered to the IFU in the same cycle as another branch prediction is stored within the queue.).

Reinman failed to teach generating branch predictions for two sequential lines in parallel during a prediction period.

However, Giacalone disclosed generating branch predictions for two sequential lines in parallel during a prediction (Giacalone: Figure 3, column 8 lines 47-67 continued to column 9 lines 1-34)(A line is a single instruction. Figure 3 shows multiple branch instructions being predicted within a single prediction period).

The advantage of using a branch predictor that can predict multiple branch instructions per cycle is that it's needed to achieve high performance in very wide superscalar processors (Giacalone: Column 2 lines 26-34). One of ordinary skill in the art would have been motivated by increased performance in superscalar processors to add the branch predictor of Giacalone to the processor Reinman. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the branch predictor of Giacalone to the processor of Reinman for the advantage of increased performance in a superscalar processor.

Reinman and Giacalone failed to teach determining if data stored in entries of a first side or a second side of a cache of a branch predictor indicates that a branch is to be taken by either of the entries, the cache being segmented into the first side and the

second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes.

However, Tran disclosed determining if data stored in entries of a first side or a second side of a cache of a branch predictor indicates that a branch is to be taken by either of the entries, the cache being segmented into the first side and the second side, where entries on said first side correspond to addresses having even-numbered indexes, and entries on said second side correspond to addresses having odd-numbered indexes (Tran: Figure 4 element 70, column 12 lines 58-67 continued to column 13 lines 1-9)(The bank of the prediction cache being accessed is determined by the least significant bit of the index into the branch prediction cache. Bank 0 stores the even indexed branch predictions and bank 1 stores the odd indexed branch predictions. The combination with Giacalone allows for multiple predictions at once to be output from both banks.)

Cache access time generally increases as a cache grows larger (Tran: Column 2 lines 43-64). Set associative caches include access time for comparing the tags of the branch instruction index, which makes the access time slower than a direct-mapped cache that has the assumption of an address match (Tran: Column 2 lines 43-64). Another advantage of direct-mapped caches is that they are cheaper to use than their set or fully associative counterparts due to the fact that fewer comparators are needed to check for correct tags. The advantages of decreased costs and decreased access latency would have motivated one of ordinary skill in the art to implement a direct-

mapped branch prediction cache. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a direct-mapped branch prediction cache into the processor of Reinman for the advantages of decreased costs and decreased access latency.

15. As per claim 2:

Reinman, Giacalone, and Tran disclosed the method as in claim 1, wherein said prediction period comprises two clock cycles (Giacalone: Figure 3, column 8 lines 47-67 continued to column 9 lines 1-34)(It's obvious to one of ordinary skill in the art that branch prediction can take more than one cycle depending on the clock speed and the complexity of the branch predictor. Thus, it's obvious to one of ordinary skill in the art at the time of the invention that the branch predictor could take two cycles.).

16. As per claim 4:

Reinman, Giacalone, and Tran disclosed the method as in claim 1, wherein an index of one of two sequential lines corresponds to an entry on said first side of said cache, and an index of another of said two sequential lines corresponds to an entry on said second side of said cache (Tran: Figure 4 element 70, column 12 lines 58-67 continued to column 13 lines 1-9)(It's inherent that in the segmented cache two sequential instructions with an odd instruction address and an even instruction address would be located in different segments of the cache.).

17. As per claim 6:

Reinman, Giacalone, and Tran disclosed the method as in claim 1.

Reinman, Giacalone, and Tran failed to teach generating branch predictions for a stream of addresses during a stall of said instruction fetch unit.

However, it would have been obvious to one of ordinary skill in the art that the only time it would have been necessary for the branch predictor to stop generating predictions is when the instruction fetch queue is full. It would have also been obvious to one of ordinary skill in the art that the instruction fetch unit could be stalled on an instruction cache miss while the instruction fetch queue was not full. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the predictor could continue predicting branches while the instruction fetch queue was stalled as long as the instruction fetch queue was not full.

18. As per claim 7:

Reinman, Giacalone, and Tran disclosed the method as in claim 1, comprising generating during a cycle a prediction for a line, said line being other than the line being fetched by said instruction fetch unit during said cycle (Reinman: Figure 5, section 4.1)(Figure 5 shows branch predictions being generated and stored in the instruction fetch queue. Thus, the predictor deals with different instructions than the instruction fetch unit during the same cycle.).

19. As per claim 8:

The specific limitation(s) of claim 8 essentially recite the specific limitation(s) of claim 7. Therefore, claim 8 is rejected for the same reason(s) as claim 7.

20. As per claim 11:

Reinman, Giacalone, and Tran disclosed the method as in claim 1, comprising delivering a branch prediction to said instruction fetch unit in the same prediction period as said branch prediction is written to said queue (Reinman: Figure 5, sections 3 and 4.1)(It's obvious to one of ordinary skill in the art at the time of the invention that the queue of figure 5 is capable of adding items and erasing items from the queue in the same cycle.)

21. As per claim 12:

Claim 12 essentially recites the same limitations of claim 1. Claim 12 additionally recites the following limitations:

A branch prediction unit (Reinman: Figure 5, section 4.1); and

An instruction fetch unit (Reinman: Figure 5, section 4.1).

22. As per claim 14:

Claim 14 essentially recites the same limitations of claim 4. Therefore, claim 14 is rejected for the same reasons as claim 4.

23. As per claim 15:

The specific limitation(s) of claim 15 essentially recite the specific limitation(s) of claim 2. Therefore, claim 15 is rejected for the same reason(s) as claim 2.

24. As per claim 16:

The specific limitation(s) of claim 16 essentially recite the specific limitation(s) of claim 11. Therefore, claim 16 is rejected for the same reason(s) as claim 11.

25. As per claim 20:

Claim 20 essentially recites the same limitations of claim 12. Claim 20 additionally recites the following limitations:

DRAM (Reinman: Figure 5)(Figure 5 shows a prefetch unit that fetches instructions from L2 cache or higher memories, such as main memory. Official notice is taken that the L2 cache or higher memory like main memory could either comprise a DRAM.).

26. As per claim 22:

Claim 22 essentially recites the same limitations of claim 20. Therefore, claim 22 is rejected for the same reasons as claim 20.

27. As per claim 23:

The specific limitation(s) of claim 23 essentially recite the specific limitation(s) of claim 2. Therefore, claim 23 is rejected for the same reason(s) as claim 2.

28. As per claim 24:

The specific limitation(s) of claim 24 essentially recite the specific limitation(s) of claim 11. Therefore, claim 24 is rejected for the same reason(s) as claim 11.

29. As per claim 25:

The specific limitation(s) of claim 25 essentially recite the specific limitation(s) of claim 8. Therefore, claim 25 is rejected for the same reason(s) as claim 8.

Response to Arguments

30. The arguments presented by Applicant in the response, received on 8/3/2007 are not considered persuasive.

31. Applicant argues "Reinman, Giacalone, and Tran failed to teach delivering said branch prediction to an instruction fetch unit during the same two clock cycle period as it is stored in said queue" for claims 1, 12, and 20.

This argument is not found to be persuasive for the following reason. This limitation hasn't been considered due to the written description rejection. The examiner is unsure if the applicant intended to try and claim the limitation from figure 4 that bypasses a branch prediction generated for the instruction 101. Regardless, the examiner notes that the inclusion of such a limitation that results in bypassing a branch prediction in figure 4 to the instruction fetch unit in the second prediction cycle would overcome the current rejections of Reinman, Giacalone, and Tran if claimed correctly.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183